High-Efficient Class F GaAs FET Amplifiers Operating with Very Low Bias Voltages for Use in Mobile Telephones at 1.75 GHz

C. Duvanaud, S. Dietsche, G. Pataut, and J. Obregon

Abstract— **High-efficient class F GaAs power FET amplifiers working with a very low drain bias voltage of 3 V required by the battery cells of portable telephones is reported. The transistor used has an optimized gate periphery of 2000 μm and a gate length of 0.7 μm. Under class F operation with a drain voltage of 3 V, it has demonstrated an output power of 24.5 dBm with 71% of power-added efficiency at the operating frequency of 1.75 GHz. Output harmonic levels lower than –25 dBc have been measured. The results obtained present the state of the art published for low bias voltage, low consumption power amplifiers required for mobile-telephone systems.**

I. INTRODUCTION

MOBILE telephones must have a long operating time. Expanding this time is achieved by a reduction of the electrical consumption. In mobile telephone systems, the output power stage requires a major part of the total dc power, so its power added efficiency must be very high.

On the other hand mobile telephones must be light weight and small. The reduction in size and weight is mainly limited by the battery cells. Low bias voltage allows the use of small size battery. Therefore, it's crucial to optimize the efficiency of the power amplifier for very low bias voltages.

Some authors have recently proposed highly efficient GaAs FET amplifiers at drain bias voltages of 4.7 V [1] and 6.2 V [2]. It has been shown that maximum operational efficiencies occure for high drain bias voltages [3], [4] and are significantly degraded for lower voltages.

In this letter, a method is proposed to increase the power-added efficiency of microwave amplifiers biased with a very low drain voltage. It requires the use of transistors with high-gate periphery and an appropriate choice of the fundamental load in conjonction with an optimum adjustment of the first two harmonic terminations presented at transistor accesses.

A. Power-Added Efficiency Improvement by Optimization of the Load Impedance at Fundamental Operating Frequency.

At microwave frequencies improvement of power-added efficiency is commonly obtained by using AB and B amplification classes. Such classes lead to an increase in efficiency due to the pulsed drain current waveform generated while the drain voltage is maintained sinusoidal. This means that harmonic voltages are terminated in short-circuits.

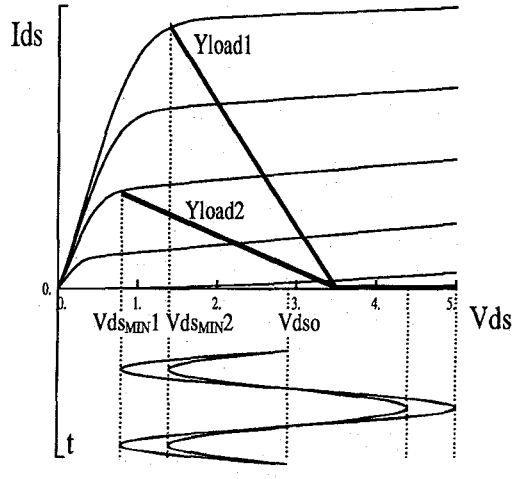

Fig. 1. Improvement of V_{ds_1} and consequently of efficiency by modifying the load line slope at fundamental operating frequency.

The efficiency depends on the ratio of the fundamental component V_{ds_1} to the average value V_{ds_0}. For a given biased voltage, maximum efficiency is achieved when the sinusoidal drain voltage reaches the lower limit between ohmic and saturation region $V_{ds_{\min}}$ (i.e., $V_{ds_{\min}} = V_{ds_0} - V_{ds_1}$). The efficiency is rapidly degraded if the drain bias voltage V_{ds_0} is near $V_{ds_{\min}}$, as illustrated by (1):

$$\text{Efficiency } \alpha \frac{V_{ds_1}}{V_{ds_0}} = 1 - \frac{V_{ds_{\min}}}{V_{ds_0}}. \tag{1}$$

A first improvement of the drain voltage ratio can be obtained by modifying the load line slope. This technique, illustrated on Fig. 1, is particularly efficient. A very inclined load line, (i.e., a low drain conductance load) leads to an increase of the peak value V_{ds_1} (i.e., decrease in $V_{ds_{\min}}$) and consequently an increase of efficiency. With such a load-line the small signal gain is improved and the temperature of the transistor channel is lowered.

However, in the previous conditions, the peak value of the drain current I_{ds_1} is reduced and the output power is significantly decreased. To overcome this major drawback, transistors with high-gate periphery must be used to maintain a high fundamental drain current.

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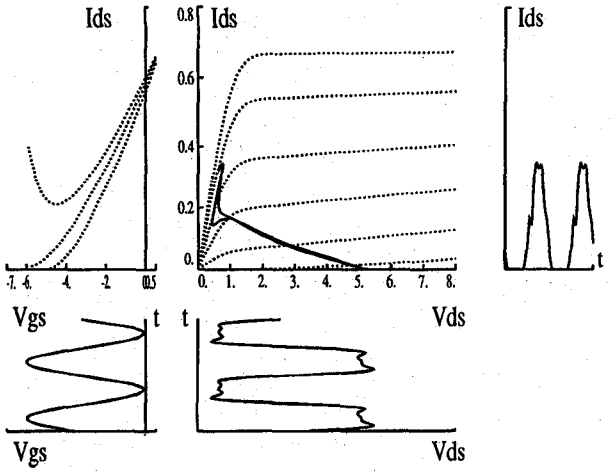

Fig. 2. Simulated waveforms and load-line required for maximum power-added efficiency I_{ds} is the drain current, V_{gs} and V_{ds} are the gate to source and drain to source control voltages.

B. Power-Added Efficiency Improvement by Optimally Loading Harmonic Components

The goal of optimally loading harmonic components is to improve the magnitude of the fundamental drain voltage component without affecting the pulse current waveform.

A *square-wave drain voltage* [5] allows the improvement of the output power (i.e., amplitude V_{ds_1}) and efficiency (i.e., ration V_{ds_1}/V_{ds_0}). This improvement is particularly significant for very inclined load line and low drain voltage.

The load impedances presented at the fundamental, second and third harmonics and leading to a high-efficient class F operation, are optimized by using a nonlinear simulator.

C. Amplifier Design and Performances.

The transistor selected for the design of this power amplifier is a FET THOMSON HP07 having a gate periphery of 2000 μm. The device selection criteria are the small signal gain and the output power available at low drain bias voltages. A classical nonlinear model used in harmonic balance simulator allows the prediction of the optimum operating conditions. The goal of the nonlinear optimization is to obtain the maximum of power added efficiency for a low-drain bias voltage of 3 V.

Fig. 2 shows the optimized dynamic load line, and the associated control voltages and drain current waveforms. The drain voltage waveform is near a square wave as it must be for class F operation. It has to be noticed that the input circuit maintains a sinusoïdal input voltage alllowing low input power.

Input and output circuit topologies are now synthesized to achieve impedance transformation from 50 ohm load to the suitable fundamental, second and third harmonic loads. Fig. 3 shows the network photograph of the proposed amplifier. The output matching network consists of three striplines. First, a short circuited stub connected to the drain port provides a suitable second harmonic impedance. This stub is near one quarter wavelength long at the fundamental frequency. It provides the drain bias and its influence upon the fundamental and third harmonic impedance is minimal.

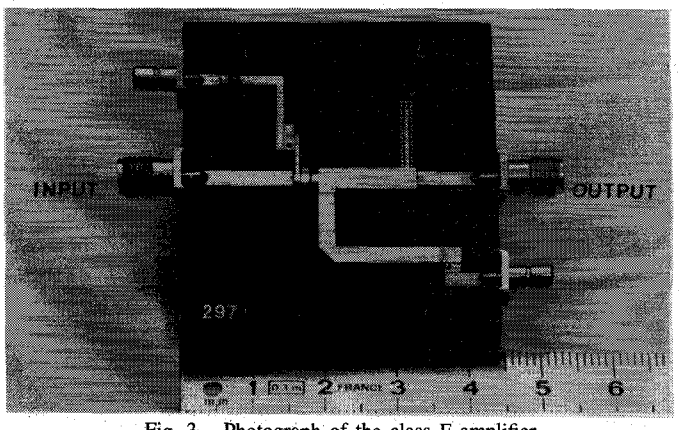

Fig. 3. Photograph of the class F amplifier.

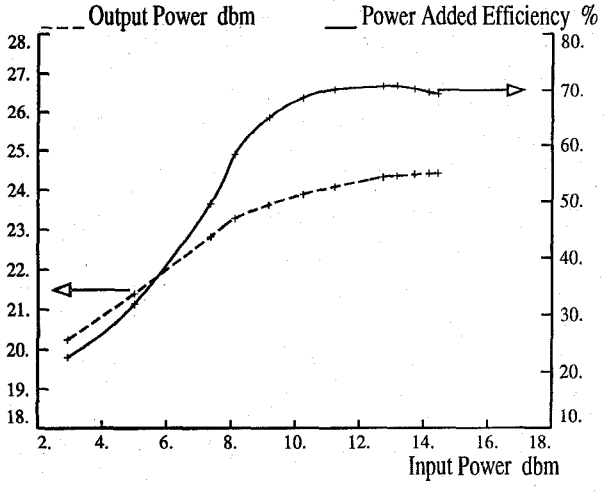

Fig. 4. Measured output power and power added efficiency versus input power at $V_{dd} = 3$ V and $V_{gg} = 3$ V.

Second, a quarter wave open stub at three time the fundamental frequency achieves a short circuit for the third harmonic. Third, a stripline transforms this short circuit into the suitable impedance at the transistor access.

Finally, the complete amplifier module was realized and tested. Drain and gate bias voltages were set respectively at +3 V and –3 V.

The output power and power-added efficiency characteristics versus input driving power at 1.75 GHz are shown in Fig. 4. The power-added efficiency of the transistor reaches 71%. The corresponding performances are the following: 24.5 dBm output power, 75% drain efficiency and 11 dB gain.

In the 80 MHz bandwidth from 1.71 to 1.79 GHz, power-added efficiency is greater than 67% for an input power of 13 dBm and 62% for an input power of 10 dBm.

The second and third harmonic levels are measured at –25 dBc and –35 dBc when the maximum power-added efficiency is obtained.

II. Conclusion

An optimized GaAs FET power amplifier has been designed and measured in the 1.75 GHz frequency range. At very low

bias voltage (–3 V; +3 V) the FET device has demonstrated a power-added efficiency of 71% and an output power of 24.5 dBm.

The key point of this optimum design are the following:

1) the use of a transistor with a high-gate periphery to maintain a high small-signal gain and a low-channel temperature;
2) the optimization of the fundamental, second and third harmonic terminations, leading to a class F operation.

To our knowledge, these results represent the best reported power-added efficiency performance obtained with very low bias voltages required for portable telephones.

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